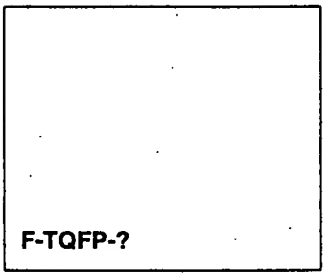
# Appendix A

# Title: Harrier-VT

# 3 Overview




The HARRIER-VT provides an highly integrated single chip solution for Voice-over-IP (VoIP) and Fax-over-IP (FoIP) applications. This solution has been tailored to serve applications such as VoIP cable modems, residential gateways, LAN telephones and LAN adapters.

The HARRIER-VT is based on Infineon's latest 32-bit TriCore architecture. This high end 32-bit single core CISC/RISC/DSP with dual MAC and SIMD capability provides a MIPS budget, which is suitable to run both, high compression/low-delay audio codecs such as G.7xx, as well as VoIP protocol stacks such as H.323, x.GCP, or SIP on a single device.

Real-time operating system support including VxWorks, Nucleus+ and PSOS provides access to a wide range of commercial and proprietary application software products.

The architecture is based on the Flexible Peripheral Interface Bus (FPI), which is interconnecting the embedded 32-bit TriCore with a variety of dedicated communication modules. Besides standard asynchronous and synchronous serial interfaces (USART, IrDA, SPI) the HARRIER-VT provides interfaces like 10/100Base-T MII Ethernet, General Purpose I/Os, time slot oriented PCM ports, and Univeral Serial Bus (USB).

The HARRIER-VT comes with a suite of software modules providing APIs, which will allow the user to effectively develop complete system solutions. The software can easily be adapted to various operating systems. Protocol software APIs allow easy integration of 3rd parties' higher layer protocol software (e.g. H.323, H.450.x, or x.GCP) as well as user's application software. Voice compression algorithms such as G.711,G.723.1 (including VAD and CNG), G.726, G.729A, G.729E, Acoustic Echo Cancellation (AEC), and DTMF can be provided in the form of linkable object code.

The evaluation kit EASY4261 will be available with engineering samples of HARRIER-VT. It may be used to exercise all functions of the HARRIER-VT and also to generate and analyze user defined IP traffic, or to capture incoming traffic for test and evaluation

| Type | Package |
|---|---|
| PEB XXXX | F-TQFP-? |

purposes. The VoIP reference kit will be provided with a complete VoIP application based on H.323 as a PCI plug-in card or stand-alone development board.

For software development and debug purposes a complete tool chain (incl. C/C++ compiler, linker, locater, profiles, assembler, and debugger) is provided by our tool partners such as Tasking, Greenhills and GNU.

## 3.1 Features

### 3.1.1 TriCore (CPU)

The TriCore is a 32-bit CISC/RISC/DSP with dual MAC and SIMD capability, optimized for real-time embedded systems. It implements a Harvard architecture with separate address and data busses for program and data memories. It has three pipelines: arithmetic, load/store, and loop control.

- High performance 80MHz CISC/RISC/DSP single core
- 32-bit load/store architecture
- Dual instruction issue
- 4 GigaByte address range ($2^{32}$)
- General Purpose Register Set:
  - sixteen, 32-bit data registers
  - sixteen, 32-bit address registers
- Shadow registers for fast context switch
- Automatic context save-on-entry and restore-on-exit for:
  - subroutine
  - interrupt
  - trap
- Two memory protection register sets
- Data types:
  - boolean
  - integer with saturation
  - bit array
  - signed fraction
  - character
  - double word integers
  - signed integer
  - unsigned integer
  - IEEE-754 single precision floating point
- Dataformats:
  - bit
  - byte (8 bits)
  - half-word (16 bits)
  - word (32 bits)

  - double-word (64 bits)
- Instruction types:
  - arithmetic
  - comparison
  - logical
  - shift
  - bit logical
  - bit field
  - packed data
  - address arithmetic
  - address comparison
  - MAC
  - coprocessor
  - branch
  - load/store
  - system
- Instruction formats:
  - 16 bit
  - 32 bit
- Addressing modes:
  - absolute
  - circular
  - bit reverse
  - base + offset
  - base + offset with pre- and post-update
- Multiply and Accumulate instructions (MAC)
  - dual 16 x 16
  - 16 x 32
  - 32 x 32
- Zero overhead loop
- Area = 5 $mm^2$ area
- Power = 1.5 mW/MHz @ 2.25V

### 3.1.2 Internal Bus (FPI)

The FPI bus is the high-speed internal bus that interconnects the TriCore core and internal peripherals. Please refer to "Peripheral Interconnect Bus, Version 3.3" for details. Implementation-specific features are listed here:

- Burst read and write of 2, 4 or 8 words
- No support for split transfers
- 32 bit address and data buses
- 1 master, 6 master/slaves and 15 slaves connected
- Limited single-master pipelining supported

### 3.1.3 Bus Control Unit (BCU)

- Handles bus arbitration between the on-chip FPI bus masters:
  - JTAG/OCDS port for debug support (TCU)
  - Peripheral Control Processor (PCP)
  - External Master Unit (XMU)
  - TriCore Program Memory Unit (PMU)
  - TriCore Data Memory Unit (DMU)
  - Transmit Data Management Unit (DMUT)
  - Receive Data Management Unit (DMUR)
- Acts as default bus slave when invalid/non-existent unit is addressed.
- Captures FPI bus error and timeout events for system debug.
- Implements algorithm to prevent request starvation due to bus domination by a high-priority master.
- Supports production testing of bus interconnect wires.

### 3.1.4 Data Memory Unit (DMU)

The HARRIER-VT contains a separate data memory unit (DMU). This unit consists of on-chip local memory, cache, and an interface to the FPI bus.

- Contains 32 kBytes of SRAM which may be configured in one of the following ways:
  - 16 kByte cache + 16 kByte scratch pad RAM (SPR)
  - 32 kByte scratch pad RAM (default after reset)
- Addressing:
  - data cache is not visible on the FPI bus.
  - scratch pad RAM is mapped in the first 16 kBytes (or 32 kBytes) of segment 13.
  - DMU configuration registers are mapped in the uppermost *256* bytes of segment 13.
- The Data cache has the following features:
  - two-way set associative
  - LRU replacement algorithm
  - line size = 128 bits
  - validity granularity = 1 valid bit per line
  - dirty bit granularity = 1 modified bit per 64-bit (2 per cache line)
  - flush, invalidate, flush + invalidate "address object" available
- The data cache objects can be individually flushed and/or invalidated to provide some support for cache coherency (to be handled by the programmer) through an instruction.
- The refill mechanism supports the following modes:
  - full refill of a cache line with burst-4 before data is accessed from/to CPU
  - no streaming

- The fetch accesses (interface to the CPU) support unaligned accesses (16-bit aligned), with a minimum penalty of one cycle for unaliged accesses crossing 2 lines (whether SPR or DCache lines).
- The data cache can not be bypassed for the cacheable segments. However, it always gets bypassed for the non-cacheable segments.
- Cache monitoring signals provided internally (not pins on the RIDER-B package):
  - cache access
  - cache hit

### 3.1.5 Program Memory Unit (PMU)

The HARRIER-VT contains a separate program memory unit (PMU). This unit consists of on-chip local memory, cache, and an interface to the FPI bus.

- Contains 16 kBytes of SRAM which may be configured in one of the following ways:
  - 8 kByte cache + 8 kByte scratch pad RAM (SPR)
  - 16 kByte cache
- Addressing:
  - instruction cache is not visible on the FPI bus.
  - scratch pad RAM is mapped in the lower half of segment 12.
  - PMU configuration registers are mapped in the uppermost 256 bytes of the lower half of segment 12.
- The instruction cache has the following features:
  - two-way set associative
  - LRU replacement algorithm
  - line size = 256 bits
  - validity granularity = 4 double-word per line
  - global invalidation support
  - not lockable
- The instruction cache can be globally invalidated to provide some support for cache coherency (to be handled by the programmer) through a write to a configuration register.
- The refill mechanism supports the following modes:
  - critical word first
  - no line wrap around
  - streaming to CPU
- The fetch accesses (interface to the CPU) support unaligned accesses (16-bit aligned), with a minimum penalty of one cycle for unaliged accesses crossing 2 lines (whether SPR or ICache lines).
- The instruction cache can be bypassed (default mode) to provide a direct fetch access from the CPU to the internal on-chip bus resources.
- Cache monitoring signals provided internally (not pins on the RIDER-B package):
  - cache access
  - cache hit

### 3.1.6 Code Memory Unit (CMU)

The CMU is a second-level program memory which connects directly to the PMU.

- 32 kBytes of SRAM.
- Acts as a pipelined synchronous memory unit.
- Synchronous read and write behavior.
- 64-bit uni-directional input and output data buses.
- Burst read support (no wrap-around supported).
- Half-word (16-bit) write granularity.
- Independent and self contained BIST circuitry.
- All read/write accesses are naturally aligned on 64bit boundary.
- All read/write accesses have programmable 0 or 1 wait state.

### 3.1.7 External Bus Unit (EBU)

The External Bus Unit (EBU), also referred to as external bus controller, provides the external interface between the HARRIER-VT and the system devices. This interface has a demultiplexed 24-bit address and 32-bit data bus. The EBU's interface connects gluelessly to various types of memories and/or peripherals, including Intel-style peripherals (separate RD and WR signals), ROMs and EPROMs, Static RAMs, and synchronous DRAMs.

The EBU acts as a bridge between on-chip FPI masters and the external bus.

- External memory configuration support summary

**Table 1**

| FPI Transaction | Demuxed Config | Muxed Config | SDRAM Config |
|---|---|---|---|
| Single (8-bit) | 8, 16, 32-bit | 8, 16, 32-bit | 32-bit |
| Single(16-bit) | 8, 16, 32-bit | 16, 32-bit | 32-bit |
| Single(32-bit) | 8, 16, 32-bit | 32-bit | 32-bit |
| Burst(2 x 32-bit) | 8, 16, 32-bit | 32-bit | 32-bit |
| Burst(4 x 32-bit) | 8, 16, 32-bit | 32-bit | 32-bit |
| Burst(8 x 32-bit) | 8, 16, 32-bit | 32-bit | 32-bit |

- Supports classic SRAM, EPROM, ROM
- Supports synchronous DRAM:
  - It will be possible, using SDRAMs with $\overline{CAS}$ latency of two, to support bursts with zero wait-states between consecutive data of the burst at 60MHz or below.
  - must use 32-bit SDRAMs.
- Supports peripherals/ASICs with Intel-style interface
- No support for synchronous Flash memories

- Demultiplexed address and data bus mode
  - byte/half-word/word accesses from FPI to external devices of 8/16/32 bit data width in any combination supported.
- Multiplexed address and data bus mode
  - byte/halfword/word access from FPI to external device of the same data width as the FPI access or bigger data width supported
  - byte access to any size device possible
  - halfword access to 16 and 32 bit devices possible
  - word access to 32 bit devices possible
- 32-bit data bus
- Data widths of 8, 16, 32 bits
- 24-bit address bus
- 4 decoded user chip select outputs
- 2 decoded emulation chip select outputs (for overlay and emulation memories)
- Little endian operation (big endian is not supported)
- Programmable timing characteristics depending on address range: memory type, address generation, wait-states, etc.
- Byte write capability (four byte control signals)
- WAIT input for additional wait-state insertion
- External bus arbitration control with master/slave operation: HOLD, HLDA, BREQ

### 3.1.8 External Master Unit (XMU)

- Chip select input pin for access to internal FPI-Bus locations using an external bus master

### 3.1.9 Peripheral Control Processor (PCP)

The PCP performs most of the tasks that are normally done by a DMA controller and CPU interrupt service routines. It off-loads the CPU from most time critical interrupts with their inherent context switches and overhead, easing the implementation of systems based on operating systems. The PCP has no need for a kernel or task management. The PCP has limited computational capabilities and an architecture that efficiently supports DMA-type of bus transactions to/from arbitrary devices and memory addresses.

- Small, programmable, interrupt-driven microcontroller for data transfer and peripheral control. Includes instructions for DMA and bit handling.
- 40Mhz operation frequency
- PRAM 256 x 64 bit (parameter memory)
- CMEM 256 x 32 bit (code memory)
- 4 Gigabyte address range
- General purpose register set:
  - eight 32-bit registers for address, data, flags, and program counter

- Separate program and data/context memories
- Data types:
  - integer
  - bit manipulation
- Instruction Types
  - DMA (COPY)
  - arithmetic
  - logical
  - flow control/branch
  - load/store/exchange
  - shift
  - bit manipulation
- 16-bit Instruction Format
- Conditional execution of arithmetic, logical, jump
- Addressing Modes:
  - absolute
  - base + offset

### 3.1.10 Timers

#### 3.1.10.1 Watchdog Timer (part of PWR unit)

The Harrier-VT Watchdog Timer provides a recovery mechanism from software or hardware failure.

#### 3.1.10.2 System Timer (STM)

The System Timer is a high-precision, long-range 56-bit timer that provides a global system time for operating systems and other purposes.

- free running 56-bit system timer
- runs with CPU clock (e.g. 100MHz)
- timing range:2 56 counts (at 100MHz overflows after 22.5 years) - capable of timing the entire lifetime of the device
- no interrupt generated on overflow
- no interrupt unit
- no control bits and control registers
- starts counting after power-on reset
- not affected by any reset except power-on reset
- special capture register (SYSTIM7) is implemented (for 56 bits capture)
- optional 56-bit capture registers can be added to record external events
- scan test ready
- Gate Count:
- Area: 0.070 $\mu m^2$ (C9)
- Max. Speed: 66 MHz (C9)

### 3.1.10.3 General Purpose Timer Unit

The general-purpose timer unit, GPTU, consists of three basic 32-bit timers. The three timers are useful in timing events, counting events, and recording events. They can either run in standalonemode or be connected together to solve more complex tasks. They can also be split into several 8-bit or 16-bit timers.

- Gate Count:
- Area: 0.316 µm 2 (C9)
- Max Speed: 66 MHz (C9)

**General Purpose Timers T0 and T1 (GPT0, GPT1)**

- 32-bit up-counting timers/counters
- max. input frequency: SYSCLK / 2
- two input pins for count option
- dedicated 32-bit reload registers with automatic reload on overflow
- can be split into individual 8-, 16- or 24-bit timers with individual reload registers
- overflow signals can be selected to generate service requests, pin output signals, and T2 trigger events
- Gate count:

**General Purpose Timer T2 (GPT2)**

- 32-bit timer/counter
- up or down count option
- max. input frequency SYSCLK / 2
- operating modes:
  - timer,
  - counter,
  - quadrature counter
- options:
  - external start/stop, one-shot operation, timer clear on external event
  - direction control through software or external event
  - two 32-bit reload/capture registers
- reload modes:
  - reload on over/underflow, reload on external event: positive, negative, or both transitions
- capture modes:
  - capture on external event: positive, negative, or both transitions
  - capture and clear timer on external event: positive, negative, or both transitions
- can be split into two 16-bit blocks
- input pins freely assignable to timer count, reload, capture, etc. trigger functions, in addition to inputs from T0 and T1 overflows
- over-/underflow signals can be used to trigger T0/T1 and to toggle output pins

- T2 events freely assignable to the service request nodes

### 3.1.11 Serial Interfaces

#### 3.1.11.1 Synchronous Serial Channel (SSC)

The High-Speed Synchronous Serial Interface, SSC0, supports full-duplex and half-duplex synchronous communication between the HARRIER-VT and other microcontrollers, microprocessors, or external peripherals. The serial clock signal can be generated by the SSC0 itself (master mode) or be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable, enabling communication with SPI-compatible devices.

- Master and slave mode operation
  - Full-duplex or half-duplex operation
- Flexible data format
  - Programmable number of data bits : 2 to 16 bit
  - Programmable shift direction : LSB or MSB shift first
  - Programmable clock polarity : idle low or high state for the shift clock
  - Programmable clock/data phase : data shift with leading or trailing edge of SCLK
- Baudrate generation from 12.5 MBaud to 190.7 Baud (@ 25 MHz module clock)
- Interrupt generation
  - on a transmitter empty condition
  - on a receiver full condition
  - on an error condition (receive, phase, baudrate, transmit error)
- Three pin interface
  - Flexible SSC pin configuration
- Scan test ready
- Gate Count: 4100 (C9-FPI)
- Area: 0.110 µm 2 (C9-FPI)
- Maximum speed: 66 MHz (C9-FPI)

#### 3.1.11.2 Asynchronous Serial Communication Interface (ASC_P)

The Asynchronous/Synchronous Serial Interfaces ASC0 and ASC1 provide seriall communication between the HARRIER-VT and other microcontrollers, microprocessors or externall peripherals. The two ASCx interfraces are identical. The ASCx operate in either asynchronous or synchronous mode.

- Full duplex asynchronous operating modes
  - 8- or 9-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baudrate from 1.5625 MBaud to 0.37 Baud ( @ 25 MHz clock f MOD )
  - Multiprocessor mode for automatic address/data byte detection

  - Loop-back capability
  - Support for IrDA data transmission/reception up to max. 115.2 KBaud
- Autobaud detection unit for asynchronous operating modes
  - Detection of standard baudrates1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400 Baud
  - Detection of non-standard baudrates
  - Detection of asynchronous modes
  - 7 bit, even parity; 7 bit, odd parity;
  - 8 bit, even parity; 8 bit, odd parity; 8 bit, no parity
  - Automatic initialization of control bits and baudrate generator after detection
  - Detection of a serial two-byte ASCII character frame
- Half-duplex 8-bit synchronous operating mode
  - Baudrate from 3.125 MBaud to 318.5 Baud (@ 25 MHz Module clock)
- Double buffered transmitter/receiver
- Interrupt generation
  - on a transmitter buffer empty condition
  - on a transmit last bit of a frame condition
  - on a receiver buffer full condition
  - on an error condition (frame, parity, overrun error)
  - on the start and the end of a autobaud detection
- Gate Count: 5000 (C9-PD)
- Area:
- Maximum speed:

### 3.1.12 Parallel Port Module (PLP)

The on-chip GPTU, ASC0, ASC1 and SSC0 peripherals are connected to an 8-bit wide I/O port with flexible programming options for general purpose I/O or peripheral input/ output functions.

RIDER-B will have three 8-bit parallel ports.

- PortO
- Port 1
- Port2

### 3.1.13 Clock

- On-chip crystal oscillator circuit
  - Allows connection of external crystal, and supporting capacitors, via a two-pin interface (XTAL1,2).
  - Supports standard crystals from {min} to {max} MHz.
  - Permits external clock source driven through the XTAL1 pin of up to {max} MHz.
- On-chip Phase-Locked Loop (PLL)
  - Clock synthesis and frequency multiplication.

- Supports internal chip clock frequencies from {min} to {max} MHz.
- Two bypass modes for forwarding an external clock into the internal clock system for chip testing.

### 3.1.14 Reset

- Several levels of chip reset are provided:
  - Power-on - resets entire chip
  - Hardware - used to synchronize board reset
  - Software - reset most of chip except key system resources (e.g. system timer).
  - Watchdog timer - recover from power down mode
- All flip-flops, except some special cases, are placed in a known state asynchronously. The reset tree is designed so that all parts of the chip will see the deassertion of reset within the same clock cycle.
- On-chip memories (i.e. SRAMs) are not reset and should be assumed to contain unknown values immediately after reset.

### 3.1.15 Power Management Unit (PWR)

The power management functions of the HARRIER-VT accommodate battery-powered devices. These functions provide long battery life and manage power loss. They also limit the peak power during turn on and reset of the HARRIER-VT in order to avoid an unnecessary Power Fault condition. There are four Power Modes: RUN, IDLE, SLEEP, and DEEP SLEEP.

- The clock tree is partitioned into several domains using clock gating cells. Each clock domain can be disabled for power saving. See "Figure 1. RIDER-B Functional Block Diagram" on page 12 for more.
- Clock domains are controlled in four ways:
  - Transparent (software invisible). Clock domain is shut off when determines that it is not needed. The clock is turned on automatically when required. This method is used in each unit for the FPI clock.
  - Idle.
  - Sleep.
  - Chip Off.

### 3.1.16 Interrupt Systems

- *256* prioritization levels which can be used among two interrupt systems: TriCore and PCP.
- TriCore interrupt control unit (ICU) with a decentralized arbitration system.
- PCP interrupt control unit (PICU) also with a decentralized arbitration system.

### 3.1.17 Emulation and Debug Support

The HARRIER-VT provides a robust on-chip debug system. Its JTAG interface conforms to IEEE 1149.1

- *Level 1:* JTAG port with FPI master capability for access to full internal address space works in conjunction with OCDS_E, BRK_IN and BRK_OUT pins.
- *Level* 2: TriCore emulation monitoring unit (EMU) using a 16-pin interface for visibility and reconstruction of code execution. Program counter and BRK_OUT pins for monitoring program execution of the PCP.
- *Extended Level 2.*. not supported on RIDER-B.
- *Level 3:* not supported on RIDER-B.

### 3.1.18 Ethernet Port

#### 3.1.18.1 Ethernet MAC

- two integrated MAC controller for 10Base-T and 100Base-FX/TX operation
- in half duplex mode, the controller implement the IEEE 802.3 Carrier Sense Multiple Access with Collision Detection (CSMA/CD) protocol.
- in full duplex mode, the controller implement the IEEE 802.3 MAC Control Layer and PAUSE operation for flow control.
- maskable notification of preset conditions
- implements counters for network management

The receive blocks accept incoming data from MII and perform the following operations:

- detection of SFD
- check CRC
- check minimum and maximum packet length
- lookup for address
- Address filtering capabilities for up to 5 MAC addresses
- Filtering for broadcast and multicast packets
- accept or reject packet.

Packets that have been accepted by the receive block are forwarded to the packet handler.

The transmit blocks forward the outgoing data from the packet handler to the MII and perform the following operations:

- generation of preamble and SFD
- generation of PADs
- generation of CRC
- generation of jam
- timer control for back-off after collision and for interpacket gap after transmission.

### 3.1.18.2 Ethernet Repeater

- provides two IEEE 802.3u compliant Media Independent Interfaces (MII) to LAN connection and external ethernet host computer.
- Supports 10Base-T and 100Base-TX/FX MII-based PHY devices
- Supports Full and Half Duplex Ethernet
- Includes MII Management Interface

## 3.1.19 PCM/HDLC Interface

Two SW configurable PCM Interfaces are provided consisting of a Port Interface, Time Slot Assigner and Protocol Machine.

**OPEN issues:**

Each PCM interface carries 32 time slots. A Frame Start signal will be provided for time slot zero. The accumulated maximum data rate will be 4.096Mbit/s.

- External CODECs or SLIC devices for the AFE
- Master and slave clock mode
- Single and double bit clock I/O
- Clock speeds configurable for 512kHz, 2,084kHz, 4,096kHz and 1,536kHz

### 3.1.19.1 Receive/Transmit Port Interfaces (XPI)

serial interface operating with gapped/non gapped serial clocks

- up to 32 channels with Nx8kbit/s (N=1...8) assigned for each PCM interface
- operation with strobed serial clocks **(future extension)**
- standard channelized mode (SCM) : 2 T1 (1.544MHz) / E1 (2.048 MHz) lines with chip internal framing function **(not supported)**
- alternate channelized mode (ACM) : 2 T1 (1.544MHz) / E1(2.048MHz) lines without chip internal framing function (E1/T1 arbitrarily portwise programmable)
- unchannelized mode (UCM) and mixed modes (SCM/UCM or ACM/UCM), UCM mode available for 2 ports
- serial data sampling/transmitting with rising/falling edge of clocks (ACM, SCM and UCM)
- ACM: sampling the receive/transmit sync pulses with rising/falling edge of clocks
- ACM: programmable TD/RD bitshift of +3/-4 bits relative to the sync pulse
- serial data multiplexable between normal and internal loop input
- supervision of frame synchronization conditions
- PCM-, HDLC-, framer- and interrupt-interface
- performance: serial clock up to 20MHz (port 0: 60MHz) ; SYSCLK up to 70 MHz
- full scan path for the SYSCLK domain

### 3.1.19.2 Time Slot Assigner (TSAT, TSAR)

- coordinates requests of 2 ports by built-in arbitration
- arbitration priority from low (port n = 0) to high (port n=1)
- channel programming by indirect access through TFPI (FPI Slave) Interface
- data output FIFO buffering for adjustment of further data processing
- programmable channel assignment per timeslot
- programmable mask per timeslot
- programmable timeslot inhibit flag per timeslot
- remote channelwise loop, one channel at a time (loop RD -> TSAR -> TSAT -> TD)
- remote portwise loop, one port at a time (loop RD --> TSAR --> TSAT --> TD)
- loop supported by a jitter attenuator, consisting of a 512 bit FIFO with slip function
- programmable "TMA1ST flag" (tmafirst flag) to identify the ' first' timeslot for TMA mode channels
- FPI target interface
- performance: SYSCLK up to 70 MHz
- scan path
- RAM (Timeslot Assigner Transmit Parameter Table: TATPT) built in selftest
- RAM (Timeslot Assigner Transmit Data Buffer: TATDB) built in selftest
- RAM (Timeslot Assigner Transmit Fifo: TATFIFO) built in selftest

### 3.1.19.3 Protocol Machine (PMT, PMR)

The two on chip HDLC Controllers are able to serve 64 logical channels which are assigned to independent PCM time slots.

- Protocols supported: HDLC, bit-synchronous PPP, octet-synchronous PPP, and Transparent modes
- full duplex operation
- Flexible scaling by dimensioning of context memory
- Per channel protocol configuration
- Configuration via Simplifed Microcontroller Interface (SMIF) registers
- Provides bit stuffing/deletion, flag detection/generation, CRC check/generation
- Aggregate throughput of 52.8 Mbit/s @ 33 MHz clock is possible

### 3.1.20 Transmit/Receive Data Management Unit (DMUT/DMUR)

- Controls linked lists for both transmit and receive direction arbitrarily assigned to the PCM/HDLC and Ethernet cores
- Provides independent internal frame buffers of 256 byte

### 3.1.21 USB Interface

The device itself may resume from suspend mode. The electrical interface and the protocol is compliant with USB specification 1.1.

- Full speed 12 Mbit/s USB device interface controller. All data transfers are initiated by the USB host
- USB Specificaton 1.1 compliant
- support of all USB device classes, including Communication Device, Audio and HID Class.
- 7 SW-configurable endpoints, in addition to the bi-directional control endpoint zero
- 3 configurations with 3 alternate settings and 8 interfaces supported
- Each non-control endpoint can be either isochronous (read-only), bulk or interrupt
- maximum packet length supported will be 1023 bytes.
- On-chip DMA support for up to 8 USB endpoints
- programmable DMA channel characteristics for each endpoint
- supports suspend and remote wake-up modes.
- Integrated USB transceiver

### 3.1.22 SW Package

Software package for VoIP reference kit includes

- Low level device driver software for on-chip communication modules
- Board support package for VxWorks
- TCP/IP stack with VoIP APIs
- APIs for H.323 and x.GCP
- Native TriCore voice codecs G.711, G.732.1 (incl. VAD and CNG), G.726, G.729A, and G.729E
- DTMF
- Acoustic echo cancellation (AEC)
- Real time T.38 fax including 14.4 bps data pump
- RTOS support for VxWorks, Nucleus+ and PSOS
- Small footprint micro kernel

### 3.1.23 Test ROM

### 3.1.24 Data-RAM with FPI Interface

## 3.2 Typical Applications

### 3.2.1 IP LAN Phone

A low-cost IP LAN phone can be built with the HARRIER-VT. **Figure 1** shows the system block diagram of an IP LAN phone based on the HARRIER-VT.

All of the interfaces inside the dashed-line rectangle required for a stand-alone IP telephone, are provided on-chip. Other system components for the IP phone include the

voice codec (Infineon's ARCOFI), two ethernet PHY devices, low cost ROM/SDRAM, display and keypad.

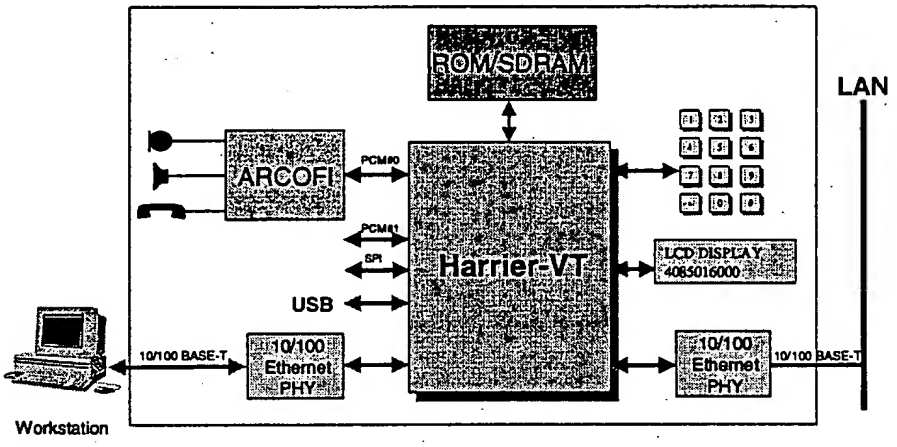



**Figure 1 An IP phone based on the HARRIER-VT.**

The IP phone is connected to the IP network via the enterprise LAN. A desktop workstation can also gain access to the LAN through the second ethernet port provided by the IP phone.

An optional USB device port is available for connecting USB devices to the IP phone for additional features.

The IrDA interface may connect PDA devices e.g. for phone directory service or email.

Real time operating system, VoIP protocols, voice codec SW, and ultilities software can be loaded into the external ROM or SDRAM.

### 3.2.2 Multi Channel VoIP Gateway

The HARRIER-VT is a scalable solution which can be configured to support up to 16 full duplex VoIP channels. The design is suitable for midsize residential gateways, multi channel Terminal-/LAN adapters or LAN linecard applications. **Figure 2** shows the functional block diagram of the basic implementation. The HARRIR-VT shipped in the 144-pin package will not support Ethernet and USB ports.

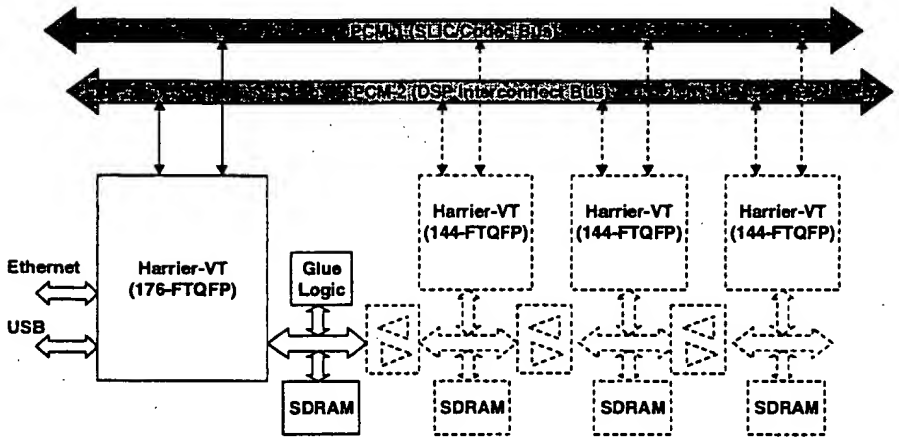



**Figure 2 A Multi-channel VoIP system**

In **Figure 2**, the HARRIER-VT (176-pin TQFP) is used as the VoIP master to the IP network providing the VoIP protocol stacks including RTP, UDP, IP and MAC access to the LAN.

Multiple HARRIER-VTs (with reduced package) can be connected to PCM-1highway which connects up to 16 SLIC/Codec devices, while the PCM-2 highway is used for data exchange between the HARRIER-VT used as a master and the N slave devices. In such a configuration, the programmer takes advantage of the HARRIER-VT as a DSP.

Using the same core in a system for both RISC and DSP, has the advantages of sharing the same kind of development tools, operating system, and application software.

When HARRIER-VT is used in DSP mode only, one HARRIER-DSP provides 100 DSP MIPS (at 80MHz) to handle 4 voice channels of full-duplex G.723.1 coding functions. The control communication and codec SW downloads between the master and the slave DSPs can be handled via the external processor bus or the SPI.

**Figure 3 Multi-channel VoIP system da<taflow**

### 3.2.3 Residential Gateway/VoIP Over Cable

The HARRIER-VT provides a highly integrated solution for cable modem VoIP applications. **Figure 4** shows an example of the cable modem with VoIP support.

**Figure 4 VoIP over cable using HARRIER-VT.**

For residential gateway applications the connection to the IP network can be provided by the HARRIER-VT as the cable modem controller.

- Up to 4 POTS phones or fax machines can be connected via the PCM interfaces.
- Depending on the VoIP coding algorithm implemented, up to four voice channels can be supported simutaneously.
- Two 10/100 Base-T ethernet ports (HUB) and a full-speed USB device interface is provided for workstation hook up.

The HARRIER-VT provides the DOCSIS-MAC with the MPEG payload and the flexibility required for implementing features such as Quality-of-Service, Service Enhancement & Feature Upgrades, and Control & Maintenance via the external bus interface. Besides this, the DSP capabilities will be used to implement the voice compression codecs on a per call basis.

When used as SDSL modem a SDSL-Transceiver connected to the PCM-Bus will be used instead of the external DOCSIS-MAC.

Gateway control protocols such as H.323, x.GCP or SIP will be implemented on the HARRIER-VT, since the RTOS is providing multi tasking capabilities.

### 3.2.4 Residential Gateway/Firewall

- Up to 4 POTS phones or fax machines can be connected via the PCM interfaces.
- One 10/100 Base-Tx/Fx port with MAC for workstation hook-up.
- One 10 Base-T port with MAC for workstation hook-up.
- Full-speed USB device interface is provided for workstation hook up.

In addition to the VoIP over cable application, encoding and decoding of the data packets is performed.

### 3.2.5 PCI Based VoIP System

A PCI VoIP adapter card can be built with the HARRIER-VT. **Figure 5** shows an example of a PCI adapter VoIP adapter card.

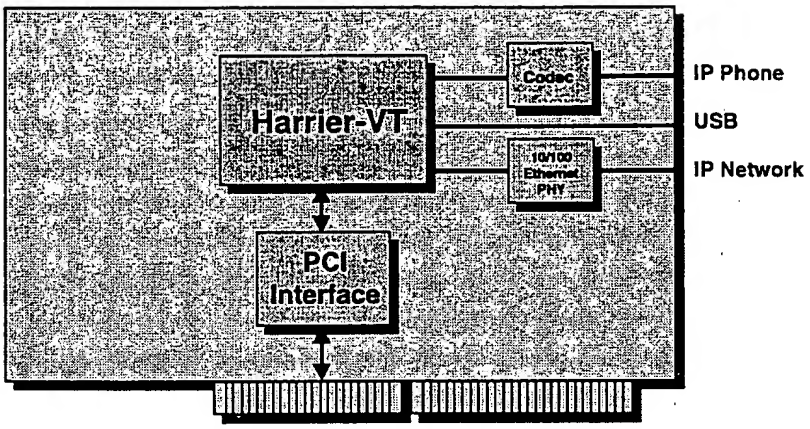



**Figure 5 PCI based VoIP adapter card.**

A basic PCI adapter card consists of the HARRIER-VT, Codecs, an ethernet PHY device, and a PCI bridge.

Without the PCI interface, the adapter card may have similar functions as a VoIP phone.

The PCI interface provides to the HARRIER-VT additional features such as sharing applications and data with the host system (therefore reducing external on-board memory) and other system modules.

Such a system is provided by Infineon as a VoIP reference card.

### 3.2.6 32bit USB-Controller

Device may be used as USB-IrDA Bridge

- 8 USB interfaces
- 7 + 1 USB endpoints
- isochronous traffic on USB
- 2 B-Channals via PCM

## 3.3 Target Criteria

### 3.3.1 Technology & Libraries

- C9N
- Four layer metalization
- Standard Cell Library:
  - Starlib (HL LIB)

– supplement to Starlib for TriCore including falling-edge DFFs (HL LIB)
- Pad Library: padlib_m3p30a_3v3? **tbd**
- Crystal Oscillator: osci_m3p80a_3v3 (PAX_ANC0 1P10M_JxN)? **tbd**
- Phase-Locked Loop: plLnderb_v1_1 (EZM, Villach, Austria)? **tbd**
- Register Files are implemented as fully synthesizable elements.

### 3.3.2 Operating Parameters

- 66 MHz (15 ns period) at typical process, worst temperature, worst voltage.
- I/O Supply. 3.3 V ±10% (3.0V to 3.6V), Low voltage TTL compatible outputs
- Core Logic: 2.5 V ±10% (2.25V to 2.75V)
- 110 $^{0}$C junction temperature (70 $^{0}$C ambient)
- Temperature range 0 $^{0}$C to + 70 $^{0}$C (optional -40 $^{0}$C to +85 $^{0}$C)
- ? Pin Quad Flat Package for F-TQFP-?, 0.5mm lead pitch **tbd**

# 5 Functional IC Description

## 5.1 Functional Overview

## 5.2 Block Diagram

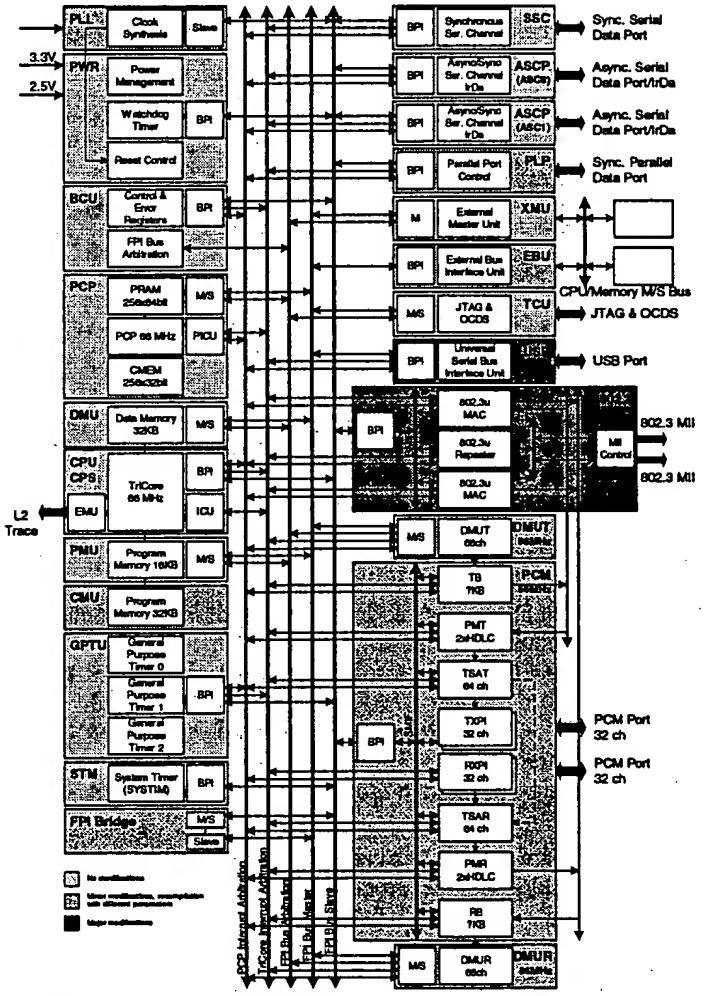



**Figure 6 HARRIER-VT block diagram.**

The HARRIER-VT block diagram is shown in **Figure 6.** It can be divided into four major functional blocks: TriCore processor core with memory and peripherals, ethernet MAC and repeater, USB and PCM/HDLC module.

## 5.3 Functional Blocks

### 5.3.1 Embedded TriCore processor core with memory and peripherals

This chapter only provides a general overview of the embedded TriCore and its peripherals. For detailed information please refer to the RIDER-B documentation.

The HARRIER-VT's embedded controller is based on Infineon's latest 32-bit TriCore architecture. The TriCore implements the computational capabilities of DSPs alongside the most optimized price/performance implementation of a RISC load/store architecture in a single core. It is well-suited for a wide variety of real-time oriented embedded control systems.

Other on-chip features of the HARRIER-VT's embedded controller include a 16-KByte instruction cache, a 32-KByte data cache, synchronous and asynchronous serial communication interfaces, a DMA/PCP, general-purpose timers, and sophisticated on-chip debug and emulation capabilities.

The embedded controller operates with a 80-MHz clock frequency. In DSP mode, the HARRIER-VT can deliver at least 100 DSP MIPS at 80 MHz.

#### 5.3.1.1 TriCore Core CPU

The CPU is an Infineon TriCore superstar implementation. The 32-bit microcontroller/ DSP core contains two major pipelines that support integer and load/store operations and a third pipeline that supports optimized DSP loop operations. The integer pipeline executes basic integer instructions, bit operations, MAC instructions, divide, and conditional data jumps. The load/store pipeline executes load/store instructions, context operations, system instructions, address arithmetic and conditional/unconditional address instructions. Both the integer and load/store pipelines share a common fetch stage that can issue one instruction to each pipeline per cycle. The multiply-accumulate (MAC) instructions are executed in a dedicated two-stage MAC pipeline containing two 16x16 multipliers.

Loop optimizations are typically found within DSP applications and can be executed within the TriCore-1 pipeline using a dedicated loop hardware cache buffer (LCB). This buffer stores the location, target, and minimal set of information required to execute any repetitive loop within the dedicated loop pipeline. Unlike a normal Branch Target Buffer hit, the loop instruction itself is not fetched and is injected from the LCB into the loop pipeline during the last execute cycle.

Context operations associated with calls, returns, and interrupt entries are all supported via a 128-bit wide data bus between the register file and the local data memory. The core also contains dedicated hardware to optimize these operations, resulting in a reduction in the overall context save time to the scratchpad SRAM.

#### 5.3.1.2 External Bus Interface Unit (EBU)

The external bus interface unit (EBU) provides a seamless interface to various external memories and peripherals, including EPROM, FLASHROM and SDRAM and "Intel-style interface" ASICs. Up to eight independent memory regions can be defined with different base address and length. Each region is associated with one chip select output and is programmable regarding bus protocol, wait states and byte ordering (little/big endian). The EBU also provides a demultiplexed 24-bit address and 32-bit data bus external interface. The data bus width can be programmed for 8-, 16-, or 32-bit wide accesses. Arbitration logic ensures that only one task is handled on the external bus at any one time and facilitates various operating modes including arbitration, external master mode, external slave mode, and stand-alone mode.

#### 5.3.1.3 External Master Unit (XMU)

This unit acts as a bridge between external bus masters and the on-chip FPI bus.

#### 5.3.1.4 On-Chip Memory

The on-chip memory of the embedded controller consists of a 16-KByte Program Memory Unit (PMU) and a 32-KByte Data Memory Unit (DMU). The PMU can be configured as 16-KByte instruction cache or 8-/8-KByte instruction cache/scratch SRAM. The DMU supports 32-KByte data cache or 16-/16-KByte data cache/scratch SRAM, Both memory blocks are supported with memory protection register sets to ensure both program and data integrity throughout system operation. Optional 32 KBytes CMU ROM for storing codeinstructions.

#### 5.3.1.5 FPI Bus and Bus Control Unit (BCU)

The FPI Bus is used for on-chip interconnections. It connects the TriCore core with the peripherals including asynchronous and synchronous serial ports and external bus controller (EBU). Moreover, the communication modules like Packet Handler and Cell Processor are connected to the FPI Bus. The FPI Bus is a demultiplexed bus with 32 address bits and 32 data bits.

The BCU manages the arbitration between the devices residing on the FPI Bus.

### 5.3.1.6 General-Purpose Timer Unit (GPTU)

The GPTU consists of three basic 32-bit timers (T0, T1, and T2). T0 and T1 are functionally the same. The features of T0 and T1 are:

- 32-bit up-counting timer/counter
- two input pins for count option
- dedicated 32-bit reload registers with automatic reload on overflow
- can be split into individual 8-, 16-, or 24-bit timers with individual reload registers
- overflow signals can be selected to generate service requests, toggle output pins, and trigger T2 events

The features of T2 include:

- 32-bit timer/counter
- up or down count option
- timer, counter, or quadrature operating modes
- external start/stop, one-shot operation, two 32-bit reload/capture registers
- reloads on underflow/overflow
- reloads on external events: positive or negative transition or both
- captures on external event: positive or negative transition or both
- can be divided into two 16-bit timer blocks
- input pins assignable to timer count, reload, capture
- events freely assignable to service request modes

### 5.3.1.7 System Timer (STM)

The system timer provides a global time base for any operating system that might be ported onto the HARRIER-VT. The main features of this timer include:

- Free-running 56-bit timer system
- Operation with maximum clock frequency
- No interrupt on overflow
- Only a power-on reset affects this timer
- Timing range is $2^{56}$ counts

### 5.3.1.8 Watchdog Timer

The watchdog timer resets the HARRIER-VT when it is not serviced in time. In addition, the timer provides a program flow trace capability and double overflow detection. Program flow detection allows the programmer to set trace points in the program that must be reached and which are checked. Double overflow detection means that if a watchdog timer reset is immediately followed by another watchdog timer reset without initializing the watchdog timer first, the part is shut down completely because a save operation is no longer possible.

If the program takes an unpredicted flow, the watchdog timer cannot be reset because the password field in the control register will not contain the expected value.

#### 5.3.1.9 Peripheral Control Processor (PCP)

The PCP is an I/O control processor that performs most of the tasks typically done by a dedicated DMA controller and CPU interrupt service routines. The PCP off-loads the CPU from time-critical interrupts, thus easing the implementation of systems based on operating systems. The architecture contains 1 KB of parameter SRAM and 1 KB of code memory. It is well-optimized to efficiently support DMA-type bus transactions to and from arbitrary devices and memory addresses. The PCP is also flexible enough to allow the implementation of a subset of the commands/instructions and operate as a simple DMA controller.

#### 5.3.1.10 Serial Serial Channel (SSC)

The HARRIER-VT has a high-speed synchronous serial programmable interface wich connects to a number of codec devices or serial EPROMs.

#### 5.3.1.11 Asynchronous Serial Communications Interface (ASCP)

The HARRIER-VT has two ASCPs that provides both full- and half-duplex asynchronous communications to other microcontrollers, microprocessors, or external peripherals. The baud rate for full-duplex asynchronous operation ranges from 1.5625 Mbaud to 0.37 baud at 25 MHz. The baud rate for half-duplex synchronous operation ranges from 3.125 Mbaud to 318.5 baud at 25 MHz. Parity, framing, and overrun error detection are provided for the asynchronous mode to ensure reliability of the data transfers. In a special synchronous mode, the ASC supports IrDA data transmissions up to 115.2 Kbaud with fixed or programmable IrDA pulse widths.

#### 5.3.1.12 On-chip Phase Lock Loop (PLL)

The Clock Module divides a master clock frequency into lower frequencies required by different units within the HARRIER-VT for operation. The module contains an on-chip oscillator and PLL circuit, permitting the HARRIER-VT to operate on a low-frequency external clock while still providing maximum performance. The PLL also provides fail-save mechanisms that detect frequency deviations and enables the execution of emergency actions in case of an external clock failure. The HARRIER-VT's flexible clocking system minimizes power consumption and reduces EMI.

#### 5.3.1.13 Resets and Interrupts

The HARRIER-VT performs the following reset functions:

- **External power-on or cold reset**
  An active-low reset pin configures the PLL and the clock circuitry through special configuration pins. It also sets an indication flag within the reset status register to inform the user about the reset type.

- **External hard or warm reset**
  An active-low reset pin serves as an external reset input and as a reset output. It can also connect to other external devices of the system in order to activate a total system hardware reset.
- **Software reset**
  The soft reset allows specific units and functions within the device to be reset without resetting the CPU and main system unit.
- **Watchdog timer reset**
  Wake-up reset from power-down mode

#### 5.3.1.14 Debug Support

Emulation and debugging support for the HARRIER-VT provides system developers with full control over the execution of the target program and allows for simple and straightforward debug of the program through observation of its executions. In-circuit emulators, bus state analyzers, and software monitors are the more regularly used debugging tools. The HARRIER-VT supports internal bus visibility, program flow tracking, and breakpoint execution through its Test Controller Unit (TCU). The TCU implements the JTAG Interface and On-Chip Debug Support (OCDS) modules.

The OCDS connects to the FPI bus with emulation hooks to the core. This configuration allows priority communication between an external debugger and the internal system. It allows access to full internal address space. It also allows the user to utilize the JTAG port of the controller via a JTAG/COM port hardware connection and to communicate with the debugger. Using this method, the user can set simple breakpoint and trigger conditions because the JTAG communicates directly with the OCDS module. Reading and writing of data memory over the JTAG is also possible. The setting of breakpoints and the realization of these breakpoints are real-time and involve little or no slippage. Real-time run control is possible at the CPU frequency using this method.

### 5.3.2 Ethernet MAC and Repeater

The HARRIER-VT includes two 10/100Base-T ethernet Media Access Controllers (MAC).

In half duplex mode, the controller implements the IEEE 802.3 Carrier Sense Multiple Access with Collision Detection (CSMA/CD) protocol. In full duplex mode, the controller implements the IEEE 802.3 MAC Control Layer and PAUSE operation for flow control. The receive block accepts incoming data from MII and performs the following operations:

- detection of SFD
- check CRC
- check minimum and maximum packet length
- lookup for address
- accept or reject packet.

Packets that have been accepted by the receive block are forwarded to the packet handler.

The transmit block forwards the outgoing data from the packet handler to the MII andperforms the following operations:

- generation of preamble and SFD
- generation of PADs
- generation of CRC
- generation of jam
- timer control for back-off after collision and for interpacket gap after transmission.

A flow control block recognizes MAC control packets and supports the PAUSE operation for full duplex links. It also supports generation of PAUSE packets, and provides timers and counters for pause control.

The command and status registers control programmable options, including the enabling or disabling of signals which notify the system when pre-set conditions occur. The status registers hold information for error handling software, and the error counters accumulate statistical information for network management software.

An ethernet repeater provides two Media Independent Interface (MII) to LAN connection and external ethernet host computer. In VoIP application, the repeater LAN interface provides to HARRIER-VT the access point to ethernet network, and at the same time, it provides the routing path to ethernet host attached to the other MII interface.

### 5.3.3 USB Interface Controller

The HARRIER-VT provides a 12 Mbit/s (Full-Speed Mode) USB device interface controller. The USB core provides maximum flexibility and performance, off-loading the CPU in such a manner that allows the user to implement value-added software features.

All USB data transfers are initiated by the USB host. The host is also suspending the device in order to save power and controls the remote wake-up. The device itself may resume from suspend mode. The electrical interface and the protocol is compliant with USB specification 1.1.

The HARRIER-VT provides eight endpoints: in addition to endpoint zero as the defaultcontrol Pipe, seven endpoints can be configured. Each of these endpoints can be of type isochronous, bulk or interrupt. Two configurations with alternate settings for multiple modes of device operation will be supported.

HARRIER-VT is designed to support f all USB device classes, including Communication Device, Audio and HID Class.

The maximum packet length supported will be 1023 bytes.

The DMA channel characteristics for each endpoint is programmable.

### 5.3.4 PCM/HDLC Module

The on chip HDLC Controller is able to serve two logical channels which are assigned to two independent PCM time slots.

In full duplex mode the controller provides HDLC mode as well as transparent mode.

The configuration of each logical channel is programmed individually. An aggregate bit rate of up to 8,192Mbit/s per direction is provided.

In HDLC mode the following tasks are performed:

- Zero Bit Insertion/Deletion
- Flag Detection/Insertion
- CRC Generation/Verification

In the transparent mode, the protocol controller performs fully transparent data transmission and reception without HDLC framing.

Two PCM interfaces are provided along with a time slot assigner which will be controlled by SW. Each PCM interface carries 32 time slots and a Frame Start signal will be provided for time slot zero. The maximum data rate will be 4.096Mbit/s.

The PCM module provides up to 16 independent 16-byte deep FIFOs for each direction.

Each PCM interface provides a single and double bit clock I/O according to master and slave mode operation.

### 5.3.5 Software Support

The overall software architecture is shown in **Figure 7** below. Besides the RTOS, such as Nucleus+, VxWorks and PSOS the HARRIER-VT comes with a set of well defined APIs for both VoIP related protocol stack software and user application specific APIs. In conjunction with native TriCore objects written in performance optimized assembly code for the voice codecs, including G.711, G.723.1, G.726, G.729A, and G.729E the programmer will have all necessary building block at hand for a specific VoIP application.

**Figure 7 VoIP Software Modules for HARRIER-VT**

Other applications such as real-time fax including V.17 data pump will be supported as well. Optional modules, such as acoustic echo cancellation (AEC), embedded HTTP server or TFTP will be available. V.90 softmodem software can be provided as a demo version for the HARRIER-VT. For a product version please contact your local Infineon sales representative.

## 5.4 Operating Modes

### 5.4.1 IP LAN Phone

The IP phone is plugged into an existing 10/100 Ethernet wall outlet. The workstation which may have occupied the outlet before, can be connected to the HARRIER-VT's second 10/100 Ethernet port.

- Both 10/100 Ethernet ports of HARRIER-VT are internally connected via a repeater.
- One 10/100 Ethernet port is connected to the IP network via the enterprise LAN.
- The second 10/100 Ethernet port enables LAN access for a desktop workstation.
- Up to 4 POTS phones or fax machines can be connected via the PCM interfaces.
- An external master may access on-chip-ressources for additional features via the external bus interface or the USB device port.
- The IrDA interface may connect PDA devices e.g. for phone directory service or email.

**Figure 8** shows the IP LAN phone dataflow. Speech is encoded by an external voice encoder which is connected to the PCM ports. Encoded voicedata is transported via the receive branch of the PCM macro to the external memory. The TriCore reads this data, performs voice compression and writes it back to external memory. After that voice packets are read from external memory by the DMUT and forwarded to the IEEE 802.3u MAC. Then the data is fed into the LAN via the on-chip repeater.

In receive direction the IEEE 802.3u MAC listens to the ethernet traffic. Upon detection of the preconfigured MAC-Address, the MAC forwards the corresponding datapacket via RB, DMUR and EBU to the external memory. The TriCore reads the payload, performs decompressession and writes it back to external memory. After that the PCM coded voice is transported via the transmit branch of the PCM macro to external voice decoder connected to the PCM ports.

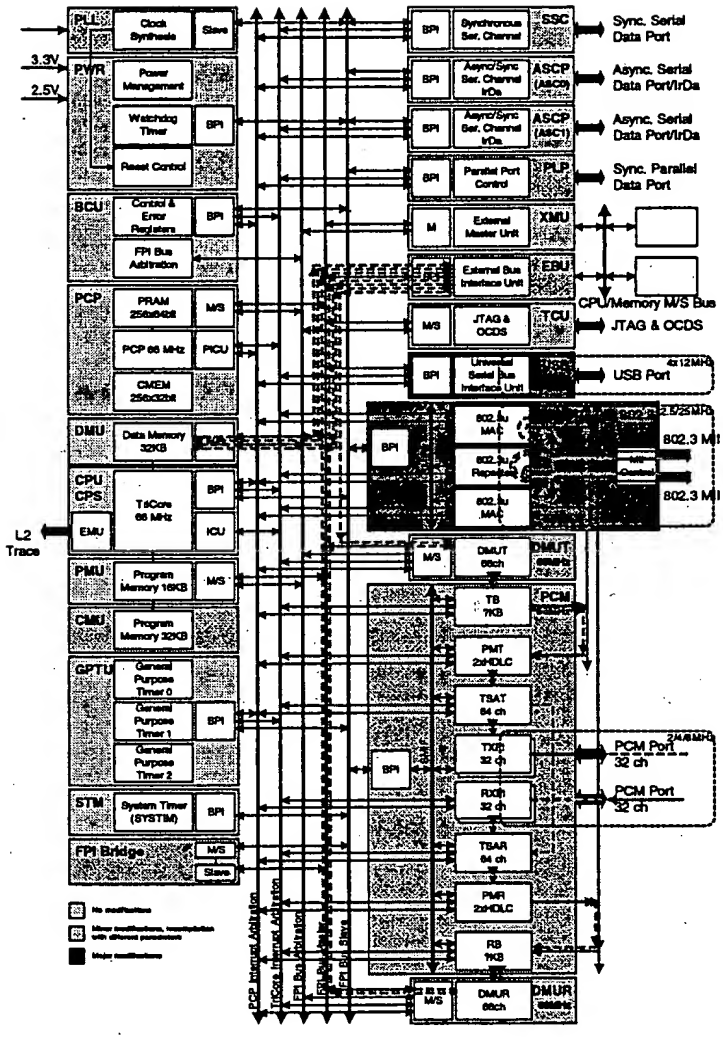



**Figure 8 IP LAN Phone dataflow**

### 5.4.2 Multi Channel VoIP Gateway

### 5.4.3 Residential Gateway/VoIP Over Cable

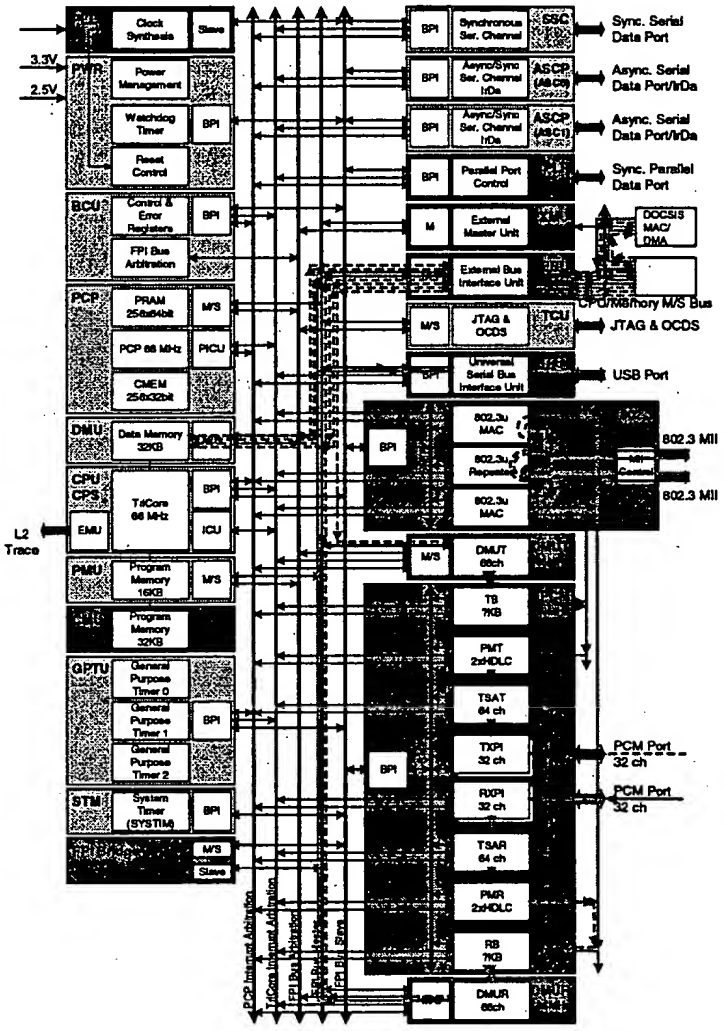



**Figure 9 Residential Gateway/VoIP Over Cable dataflow**

The dataflow for this application is shown in **Figure 9**. The external DOCSIS MAC copies received voice and data packets to the external memory. Voice packets are then read by the TriCore, decompressed and written back to external memory. After that the data is read by the transmit branch of the PCM module and forwarded to an external PCM encoder connected to the PCM port. Data packets are either moved from external memory to the USB port or via DMUT, TB and the IEE 802.3u MAC to the LAN.

In transmit direction encoded voice is forwarded via the receive branch of the PCM module to the external memory. The TriCore reads this data, does the compression and writes it back t the external memory. Data packets received from the MAC are forwarded via RB, DMUR and EBU to external memory. These voice and data packets are ready to be read by the external DOCIS MAC.

### 5.4.4 Residential Gateway/Firewall

**Figure 10** shows the corresponding dataflow. It is basically the same as in the application above. After reception by the DOCSIS MAC data packets are read from external memory, encoded by the TriCore and written back to external memory before they are forwarded to the USB or ethernet interface. In transmit direction data packets written to external memory from USB or ethernet are encoded by the TriCore before transmittion via the DOCSIS MAC.

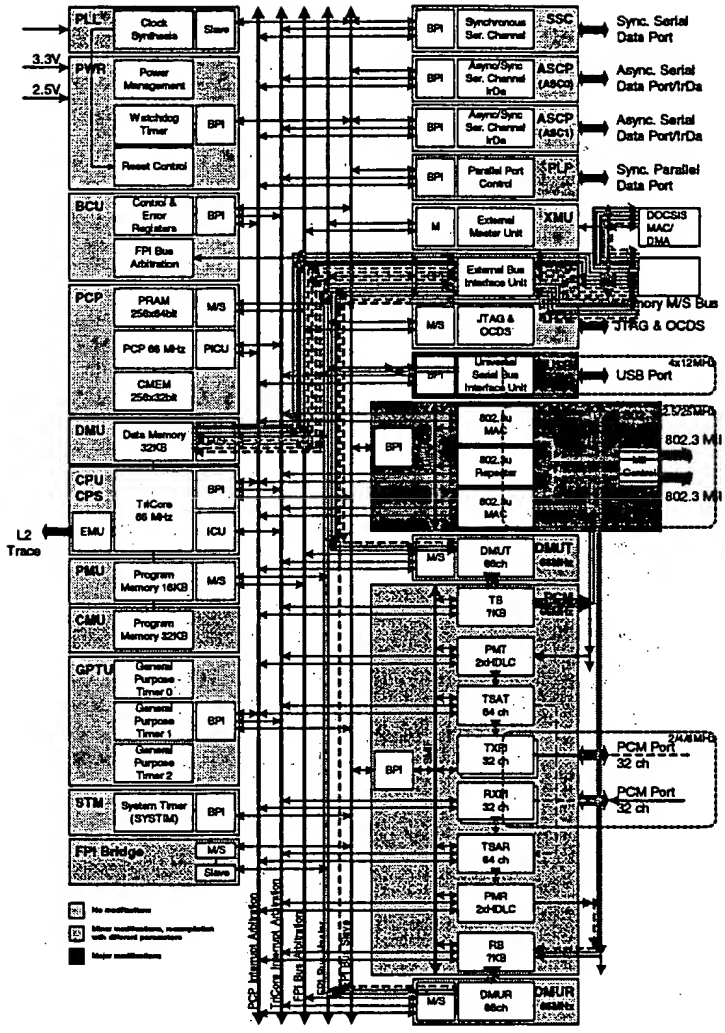



**Figure 10 Residential Gateway/Firewall dataflow**

### 5.4.5 PCI Based VoIP System

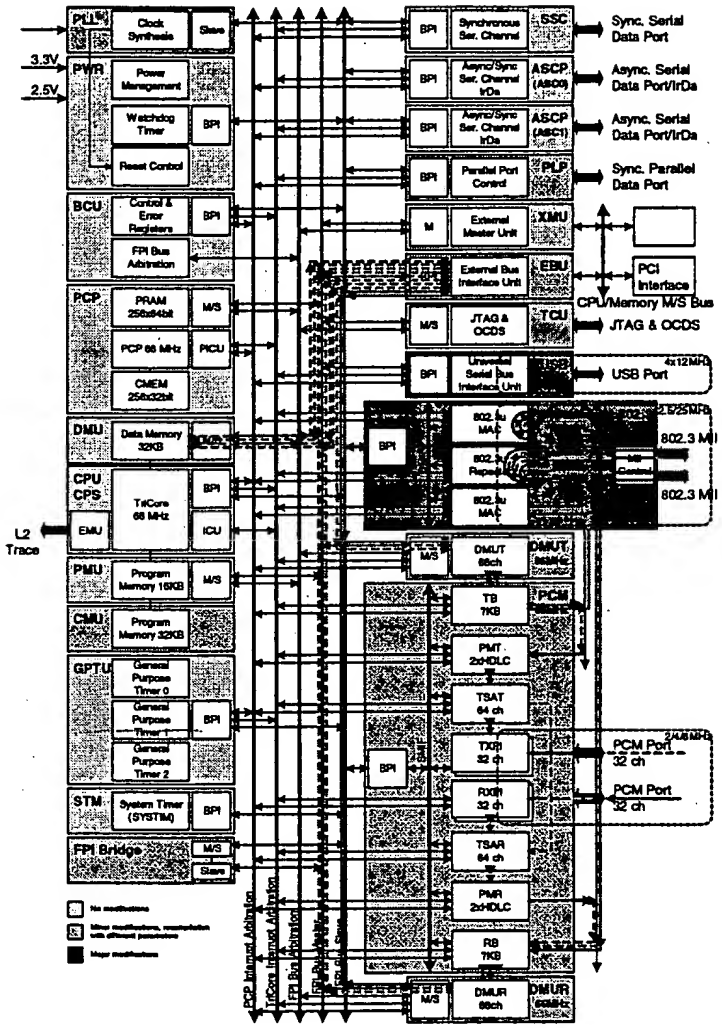



**Figure 11 PCI Based VoIP System dataflow**

### 5.4.6 32bit USB-Controller

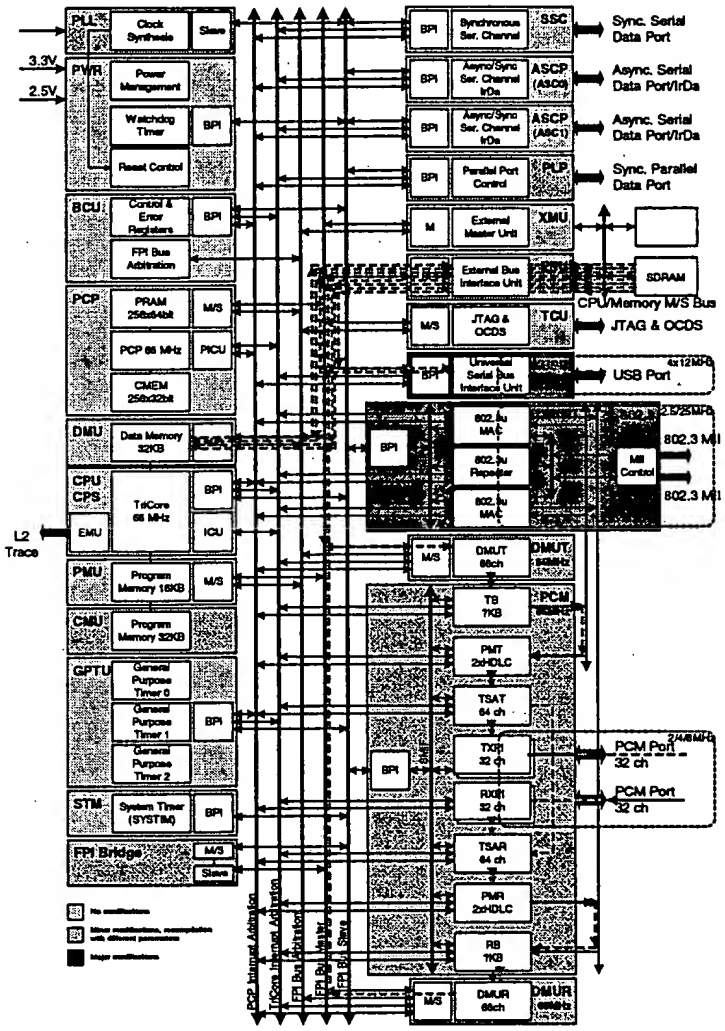



**Figure 12 32bit USB-Controller dataflow**

The PCM port is connected to an external voice codec. In transmit direction the voice samples are written through the receive branch of the PCM block to the external memory. The TriCore reads these packets, does voice compression and writes them

back to the external memory. After that the voice packets ar ready to be read by the USB master connected to the USB port. In receive direction isochronous USB voice packets are written to the external memory. The packets are then read by the TriCore, decompressed and written back. Finally the voice samples are forwarded to the PCM port through the transmit branch of the PCM macro.